

FIG. 20

- [0054] FIG. 20A is a SEM micrograph of an example of a prior art type of device of the kind shown in FIG. 2 wherein polysilicon residue is left by an insufficient overetch due to a shorter polysilicon RIE.
- [0055] FIG. 21 shows a yield chart for word line electrical continuity.

DETAILED DESCRIPTION

- [0056] FIG. 3 shows a device 10 in accordance with this invention, which is a modification of the prior art device 9 of FIG. 2. While keeping thick polysilicon layer 18 at the base of the polysilicon-barrier-metal gate electrode stack 27 in the logic circuitry in the support region, an additional thin layer of polysilicon 20 has been introduced into the word lines 26A-26C as well as stack 27. In the word line stacks 26A-26C, the additional polysilicon layer 20 serves to promote adhesion between a metallic conductor multilayer coating 21, preferably comprising a lower WN film below a W layer or the like as described below, and isolation structures, i.e. ATO layers 15 and sidewall spacers 25, and to improve electrical continuity of word line stacks 26A-26C by conformally covering imperfections in those isolation structures which otherwise could not be covered and/or filled by a metallic layer resulting in a dis-

thickness of polysilicon layers 18 and 20 should be larger than the thickness of metallic conductor multilayer coating 21 multiplied by the overetch factor. Small overetch factors are highly desirable because they allow for thinner layers 18 and 21, smaller overall gate stack height, and, consequently, reduced capacitance and stack aspect ratio of the gate stack.

[0117] The applicants have also found that a reduction of the metallic conductor multilayer coating 21 overetch can lead to inadvertent electrical shorts due to an incomplete removal of conductive material around non-conformal topographical features such as steps.

FIG. 20
[0118] ~~FIG. 20A~~ is a SEM micrograph showing a plain tilted view of an example of a prior art type of gate electrode stack 9 of FIG. 2 with polysilicon residue left by an insufficient overetch due to a shorter RIE overetch. FIG. 20A shows the gate polysilicon layer 18, WN/W layers 21 and CN layer 22 and the chromium (Cr) provided for decoration.

FIG. 20
[0119] ~~FIG. 20A~~ provides a SEM micrograph with a tilted view of a support region with 25,000 times magnification. The combined thickness of polysilicon layers 18 and 20 is about two times larger than that of the metallic layer 21. The amount of the metallic conductor multilayer coating